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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/044,162	01/11/2002	Shahram Mostafazadeh	NSC1P225R	3102
22434	7590	05/17/2005	EXAMINER	
BEYER WEAVER & THOMAS LLP			PHAM, THANH V	
P.O. BOX 70250			ART UNIT	PAPER NUMBER
OAKLAND, CA 94612-0250			2823	

DATE MAILED: 05/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>
	10/044,162	MOSTAFAZADEH ET AL.
	<b>Examiner</b>	<b>Art Unit</b>
	Thanh V. Pham	2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

1) Responsive to communication(s) filed on 04 May 2005.  
 2a) This action is FINAL.                    2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

4) Claim(s) 1-10 is/are pending in the application.  
 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
 5) Claim(s) \_\_\_\_\_ is/are allowed.  
 6) Claim(s) 1-10 is/are rejected.  
 7) Claim(s) \_\_\_\_\_ is/are objected to.  
 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

1) Notice of References Cited (PTO-892)  
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)  
 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
 Paper No(s)/Mail Date \_\_\_\_\_.  
 4) Interview Summary (PTO-413)  
 Paper No(s)/Mail Date \_\_\_\_\_.  
 5) Notice of Informal Patent Application (PTO-152)  
 6) Other: \_\_\_\_\_.

## DETAILED ACTION

### *Response to Amendment*

1. The Declaration filed on 05/04/2005 under 37 CFR 1.131 is sufficient to overcome the Melton et al. reference, the finality of the last Office action mailed 03/31/2005 is withdrawn, the new finality is made in this Office action.
2. Applicant's arguments with respect to claims 1-10 have been considered but are moot in view of the new ground(s) of rejection.

### *Claim Rejections - 35 USC § 103*

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.
4. Claims 1-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Djennas et al. US 5,474,958 in combination with Ogawa et al. US 5,252,855 and Pace US 5,904,499. Reliance on Melton et al. is withdrawn because the reference is cumulative of the teaching of Djennas et al.

The Djennas et al. reference discloses methods for making semiconductor device having no die supporting surface. Throughout the description of the embodiments, the Djennas et al. reference discloses "there may be other embodiments of the present invention which are not specially illustrated", col. 2, lines 65-67, the

"placement and geometry of the leads on the lead frame and of the conductive traces on the substrate are not restricted by the present invention" col. 12, lines 1-3;

*Re claims 1 and 7*, in the first embodiment, fig. 4-6, the Djennas et al. reference discloses a method for making semiconductor device having no die supporting surface comprising:

forming a flat lead frame including a plurality of leads extending radially from a central opening, "no tie bars, such as shown in FIG. 1 of the prior art", col. 4, lines 10-11, the lead frame *inherently* having opposing upper and lower surface;

the lead frame and an integrated circuit die are mounted onto a supporting work holder, "the stiffness of the wire bond 26 is sufficient to hold the semiconductor die 22 in place during handling, transport, and most importantly, the molding process", col. 4, lines 37-40;

forming a plastic casing over an upper surface of the die and the upper surface of the lead frame;

the die *inherently* includes a plurality of die bond pads so that "the active surface of the semiconductor die 22 is wire bonded to the plurality of conductors 12", col. 4, lines 20-22 (*re claims 2-3*).

The first embodiment does not use removable tape.

In the sixth embodiment, a "removable tape 148 is affixed to the bottom surface of the substrate 100 including the die cavity 102 ... the tape 148 provides a temporary die supporting surface whereupon the semiconductor die 22 is placed", col. 9, lines 6-12;

the step of forming the plastic casing comprises molding plastic onto the upper surfaces of the die and the substrate, fig. 19 (*re claim 6*);

“the removal of the tape 148 from the bottom of the substrate 100 after the step of molding”, col. 9, lines 49-51, whereby exposed portions of the substrate form the only externally accessible I/O contacts for the package, fig. 20.

It would have been obvious to one of ordinary skill in the art at the time of the invention to provide the lead frame of the first embodiment with the removable tape of the sixth embodiment as suggested by Djennas et al. because the removable tape would provide support during handling, transport, and most importantly, the molding process (col. 9, lines 6-12), no vacuum needed for the wire bonding process (col. 9, lines 28-29) and to prevent flash during the molding process (col. 9, lines 39-41).

Alternatively, it would have been obvious to one of ordinary skill in the art at the time of the invention to provide the sixth embodiment with the typical lead frame of the first embodiment without a die supporting surface because the lead frame without supporting surface would be selected in accordance with the method of forming flat device to prevent cracking at such locations 30, 32 and 34 as taught by Djennas et al. (col. 1, line 58 – col. 2, line 15, col. 5, lines 13-15).

The Djennas et al. reference discloses substantially all of the instant invention and ignores how the conventional lead frame is formed.

The Ogawa et al. reference discloses a method, figs. 1 and 3, using a lead frame without attached bumps wherein “a lead frame for use in a semiconductor package is

made by punching with a pressing machine or by etching of a plate material", col. 1, lines 13-15 (*re claims 4-5*).

It would have been obvious to one of ordinary skill in the art at the time of the invention to provide the method of Djennas et al. with the lead frame of Ogawa et al. because the lead frame of Ogawa would provide the package of Djennas et al. with improved reliability (Ogawa's col. 1, line 10). The method of forming the lead frame is well known in the art as taught by Ogawa.

With this combination, the exposed portions of the leads form the only externally accessible I/O contacts for a resulting integrated circuit package, these only externally accessible I/O contacts at the lower surfaces of the leads would be used to solder the package to the circuit board to electrically connect the package to the circuit board. Further, the Djennas reference teaches "the external portion of the leads can be in any surface mount or through hole configuration... a heat sink may be attached to the inactive surface of the semiconductor die in any of the embodiments provided that the inactive surface is at least partially exposed... other methods of attaching the device to a board besides solder balls are anticipated as being suitable in practicing the invention" (col. 12). Furthermore, the Pace reference claims that its method is better than "conventional 'cavity up' packages where the heat has to be removed through the substrate into a printed circuit board", col. 6, line 64 to col. 7, line 3. It means that the mounting the package on a circuit board such that it is in directed contact with a heat sink formed on the circuit board is well known to those skills in the art.

It would have been obvious to one of ordinary skill in the art at the time of the invention to provide the method of the combination with the board that has a heat sink so that when the package was mounted on the circuit board its die's lower surface would contact the 'heat sink' as a mean to conduct heat out of the package. The use of heat sink (the substrate) in the "cavity up" packaging process is well known to those skilled in the art as taught by Pace.

***Conclusion***

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.
6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh V. Pham whose telephone number is 571-272-1866. The examiner can normally be reached on M-T (6:30-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

*wp*

05/12/2005

*George Fourson*  
George Fourson  
Primary Examiner